CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A process for fabricating a semiconductor device comprising:

providing a substrate;

forming a conductive layer over the substrate;

forming a plurality of gate-like structures protruding from the conductive layer, each gate-like structure having a first gate width and sidewalls and is separated from each adjacent gate-like structure by a first gap width;

forming spacers on the sidewalls of the gate-like structures to thereby reduce said first gap width between adjacent gate-like structures; and

etching the conductive layer using the gate-like structures and spacers as masks to form a plurality of conductive gate structures each having a second gate width approximately corresponding to the first gate width plus the width of two of said spacers, wherein adjacent ones of said conductive gate structures are separated from each other by a second gap width approximately corresponding to the first gap width minus the width of two of said spacers.

2. The process according to claim 1, wherein forming the plurality of gate-like structures comprises:

forming an insulating layer over the conductive layer, and

patterning the insulating layer to form a plurality of insulator caps, wherein the plurality of insulator caps are the plurality of gate-like structures,

wherein the conductive layer is etched using the insulator caps and spacers as hard masks to form the plurality of conductive gate structures.

3. The process according to claim 1, wherein forming the gate-like structures comprises

depositing a resist layer on the conductive layer,

patterning the resist layer according to a desired arrangement of gates to be formed from the conductive layer, and

partially etching through the conductive layer to form the gate-like structures,

and wherein etching the conductive layer to form the conductive gates results in removal of the remainder of the conductive layer except for the regions defined by the gate-like structures and the regions on the partially etched conductive layer covered by the spacers.

4. The process according to claim 3, wherein

the partial etching of the conductive layer with the patterned resist thereon results in the gate-like structures being formed as a plurality of substantially unetched regions of the conductive layer,

the partial etching of the conductive layer reduces the thickness of the conductive layer to approximately one-half of the original thickness thereof,

except at the substantially unetched regions defining the gate-like structures, and

etching the conductive layer to form the conductive gates results in removal of the remainder of the conductive layer except for the regions defined by the gate-like structures and the regions on the partially etched conductive layer covered by the spacers.

5. The process according to claim 1, further comprising:

lightly doping a region between two adjacent ones of the plurality of conductive gate structures.

6. The process according to claim 5, wherein lightly doping the region between two adjacent conductive gate structures is performed by implanting into the region a concentration of ions in the range of about $3 \cdot 10^{11}$ ions/ cm^2 to about $1 \cdot 10^{14}$ ions/ cm^2.

7. The process according to claim 6, wherein lightly doping the region between two adjacent conductive gate structures is performed by implanting into the region a concentration of ions in the range of about $1 \cdot 10^{12}$ ions/ cm^2 to about $1 \cdot 10^{13}$ ions/ cm^2.

8. A process for fabricating a semiconductor device comprising:

providing a substrate;

forming a conductive layer over the substrate;

patterning the conductive layer to form a plurality of gate structures; and

lightly doping a region between two adjacent ones of the plurality of gate structures.

9. The process according to claim 8, wherein lightly doping the region between two adjacent gate structures is performed by implanting into the region a concentration of ions in the range of about $3 \cdot 10^{11}$ ions/ cm^2 to about $1 \cdot 10^{14}$ ions/ cm^2.

10. The process according to claim 9, wherein lightly doping the region between two adjacent gate structures is performed by implanting into the region ions in the range of about $1 \cdot 10^{12}$ ions/ cm^2 to about $1 \cdot 10^{13}$ ions/ cm^2.

11. A semiconductor device comprising:

a substrate; and

at least two gate structures formed in a single layer on said substrate, said gate structures being spaced apart by a gap measuring in the range of approximately 100 Angstroms to approximately 2000 Angstroms.

12. The semiconductor device according to claim 11, wherein said gate structures are spaced apart by a gap measuring in the range of approximately 300 Angstroms to approximately 1000 Angstroms.

13. The semiconductor device according to claim 11, wherein the at least two gate structures are formed of a conductive material selected from polysilicon, silicide, metal, polysilicon and silicide, and polysilicon and metal.

14. The semiconductor device according to claim 11, wherein the gate structures are transistor gates in a CCD imager.

15. The semiconductor device according to claim 11, wherein the gate structures are transistor gates in a CMOS imager.

16. The semiconductor device according to claim 15, wherein the CMOS imager has one of a 3T, 4T, 5T, 6T or 7T architecture.

17. The semiconductor device according to claim 15, wherein the transistor gates include at least two of a photogate, a transfer gate, a reset gate, a source follower gate, a row select gate, and a storage gate.

18. The semiconductor device according to claim 11, further comprising a lightly doped region between two adjacent ones of the gate structures.

19. The semiconductor device according to claim 18, wherein the lightly doped region is implanted with ions in the range of about $3 \cdot 10^{11}$ ions/ cm^2 to about $1 \cdot 10^{14}$ ions/ cm^2.

20. The semiconductor device according to claim 19, wherein the lightly doped region is implanted with ions in the range of about $1 \cdot 10^{12}$ ions/ cm^2 to about $1 \cdot 10^{13}$ ions/ cm^2.

21. The semiconductor device according to claim 18, wherein the at least two gate structures are transistor gates for a CCD imager.

22. The semiconductor device according to claim 18, wherein the at least two gate structures are transistor gates for a CMOS imager and the two adjacent gate structures having the lightly doped region therebetween are selected from among a photogate, a transfer gate, a reset gate, a source follower gate, a row select gate and a storage gate.

23. The semiconductor device according to claim 22, wherein the two adjacent gate structures having the lightly doped region therebetween include a photogate and either a transfer gate or a storage gate.

24. The semiconductor device according to claim 22, wherein the two adjacent gate structures having the lightly doped region therebetween are n-channel gates and the lightly doped region therebetween is an n-type region.

25. The semiconductor device according to claim 22, wherein the two adjacent gate structures having the lightly doped region therebetwen are p-channel gates and the lightly doped region therebetween is a p-type region.

26. A semiconductor device comprising:

a substrate;

a plurality of conductive gates formed over the substrate; and

a lightly doped region in the substrate between two adjacent ones of the plurality of conductive gates.

27. The semiconductor device according to claim 26, wherein the lightly doped region is implanted with ions in the range of about $3 \cdot 10^{11}$ ions/ cm^2 to about $1 \cdot 10^{14}$ ions/ cm^2.

28. The semiconductor device according to claim 27, wherein the lightly doped region is implanted with ions in the range of about $1 \cdot 10^{12}$ ions/ cm^2 to about $1 \cdot 10^{13}$ ions/ cm^2.

29. The semiconductor device according to claim 26, wherein the plurality of conductive gates are transistor gates for a CCD imager.

30. The semiconductor device according to claim 26, wherein the plurality of conductive gates are transistor gates for a CMOS imager and the two adjacent conductive gates having the lightly doped region therebetween are selected from among a photogate, a transfer gate, a reset gate, a source follower gate, a row select gate and a storage gate.

31. The semiconductor device according to claim 30, wherein the two adjacent conductive gates having the lightly doped region therebetween include a photogate and either a transfer gate or a storage gate.

32. The semiconductor device according to claim 30, wherein the two adjacent conductive gates having the lightly doped region therebetween are n-channel gates and the lighly doped region is an n-type region.

33. The semiconductor device according to claim 30, wherein the two adjacent conductive gates having the lightly doped region therebetween are p-channel gates and the lighly doped region is an p-type region.

34. An image processing apparatus comprising:

an image sensor for detecting an image and outputting image signals corresponding to the detected image; and

an image processor for processing the image signals outputted from the image sensor,

wherein the image sensor comprises:

a substrate; and

at least two gate structures formed in a single layer on said substrate, said gate structures being spaced apart by a gap measuring in the range of approximately 100 Angstroms to approximately 2000 Angstroms.

35. The image processing apparatus according to claim 34, wherein the gate structures are spaced apart by a gap measuring in the range of approximately 300 Angstroms to approximately 1000 Angstroms.

36. The image processing apparatus according to claim 34, wherein the image sensor is a CCD image sensor.

37. The image processing apparatus according to claim 34, wherein the image sensor is a CMOS image sensor.

38. The image processing apparatus according to claim 34, further comprising a lightly doped region between two of the gate structures.

39. An image processing apparatus comprising:

an image sensor for detecting an image and outputting image signals corresponding to the detected image; and

an image processor for processing the image signals outputted from the image sensor,

wherein the image sensor comprises:

a substrate;

a plurality of conductive gates formed over the substrate; and

a lightly doped region in the substrate between at least one pair of adjacent conductive gates.

40. A processing system, comprising:

a processor for receiving and processing image data; and

an image data generator for supplying image data to the processor, the image data generator comprising

an image sensor for obtaining an image and outputting an image signal,

an image processor for processing the image signal, and

a controller for controlling the image sensor and the image processor,

wherein the image sensor comprises:

a substrate, and

at least two gate structures formed in a single layer on said substrate, said gate structures being spaced apart by a gap measuring in the range of approximately 100 Angstroms to approximately 2000 Angstroms.

41. The processing system according to claim 40, wherein the image sensor is a CCD imager.

42. The processing system according to claim 40, wherein the image sensor is a CMOS imager.

43. The processing system according to claim 40, further comprising a lightly doped region between at least one pair of adjacent gate structures.

44. A processing system, comprising:

a processor for receiving and processing image data; and

an image data generator for supplying image data to the processor, the image data generator comprising

an image sensor for obtaining an image and outputting an image signal,

an image processor for processing the image signal, and

a controller for controlling the image sensor and the image processor,

wherein the image sensor comprises:

a substrate;

a plurality of conductive gates formed over the substrate; and

a lightly doped region in the substrate between two adjacent ones of the plurality of conductive gates.